Building Blocks for 3D Integrated Circuits:
Single Crystal Compound Semiconductor Growth and Device Fabrication on Amorphous Substrates

by

Debarghya Sarkar

A Dissertation Presented to the
FACULTY OF THE USC GRADUATE SCHOOL
UNIVERSITY OF SOUTHERN CALIFORNIA
In Partial Fulfillment of the
Requirements for the Degree
DOCTOR OF PHILOSOPHY
(Electrical Engineering)

May 2020

To all of material and abstract consciousness
that have shaped me until today

Acknowledgments

It was late August in 2014, when I started my Ph.D. program at USC. Five and half years since then (at the time of writing this dissertation), with over 2500 emails and numerous Slack messages, and uncounted hours of working together in the lab ranging from building custom pieces of equipment to performing experiments or brainstorming ideas, I have been extremely privileged to have shared a very close and unique relationship with Professor Rehan Kapadia. Being a first generation Ph.D. student (I was a week late to claim myself to be the first student!), I have seen first-hand, the extreme hard work of my advisor in his initial years as a faculty member, and have directly and indirectly been inspired by that. I would forever cherish those days when he has played the role of a senior grad student, post-doc and professor – all together – when he literally held our hands and taught us the fine details of every aspect of research while inspiring us of being able to visualize the bigger picture and gradually pushing us towards being independent researchers. Dotted with multitude of embarrassingly stupid mistakes all throughout the years including some that resulted in very trying situations, I've amazingly found a very gentle supportive person in him during these times. My biggest critic during these years, one who knows my biggest weaknesses inside-out and have helped me identify and address them, I'll be forever grateful to Professor Kapadia for what I've received from him. In many ways, he has gone much beyond what I would expect from a research advisor, and has helped me progress. Not just conducting research, but the art of communicating the results well – through writing and through oral presentations – I would always appreciate his efforts to try to make me a holistic research personality. Ranging from collaborating with several groups, to encouraging me to attend multiple conferences for presenting my research and building my professional network, my advisor has taken utmost care to help me gain visibility in the research community. And I can go on and on, but it would possibly still not be sufficient to describe his contributions to turn me from an ugly duckling to a swan. I don't think I have given enough justice to his efforts in making me a beautiful one, but I'll continue to strive to be one, some day. Thank you very much, Professor.

In addition to Professor Kapadia, there were several other professors who also played different significant roles in my Ph.D. career, and I would like to acknowledge them next.

I'll be forever indebted to Professor Michelle Povinelli, for her instrumental role in having me selected as a Ph.D. student with incoming fellowship at USC. I literally owe my very Ph.D. opportunity at USC, to her. Professor Jayakanth Ravichandran is someone whom I shared a very cordial relationship with. After my direct advisor, he was the one who seemed to always understand me very well, and I am fortunate to having been able to discuss many of my professional (and personal) issues with him on multiple occasions. A stalwart for his research contributions for over five decades, and yet a very nice and caring personality, and still so eager to learn new things and simultaneously share his immense knowledge to mentor our collaboration

– is how I would remember Professor Paul Daniel Dapkus. A big thanks to Professor Steve Cronin for allowing us to use his photoluminescence setup throughout my Ph.D. That tool definitely had a huge impact on my Ph.D. progress.

Special thanks to Professor Arka Majumdar (at University of Washington) and Professor Megan McCain (from USC Biomedical Engineering) for the collaborations I was a part of, and for the mentorship I've received from them at different stages.

Professor Wei Wu, whose always-cheerful greeting would necessarily make me smile even on the most troubled days; Professor Han Wang, whose lab equipment I've also used at times; Professor Willie Ng and Dr. William Schroeder, whom I learnt quite a bit of optical components handling from, in my initial days; Professor Anupam Madhukar, who with his scrutinous queries would encourage me to think more deeply about my research and will always serve an inspiration for me in the way I may teach in future; Professor Anthony Levi, Professor Aluizio Prata, Professor Armand Tanguay, whose courses have helped me create a strong foundation to build my scientific understanding and critical analysis; and many others whom I've received mentorship on multiple occasions – Professor Andrea Armani, Professor Constantine Sideris, Professor Hossein Hashemi, Professor Bhaskar Krishnamachari – and the list goes on.

A good majority of my time was spent in the USC cleanroom: thanks to Dr. Donghai Zhu and Alfonso Jimenez for their efforts in keeping everything running. Special thanks to Megan Utley.

The ability to use the JPL MDL cleanroom was an absolute boon. I would appreciate Dr. Frank Greer's efforts for having me get access to a whole spectrum of tools there, and also introducing me to a number of brilliant scientists who work there from whom I've also learnt a lot.

Next, I would like to acknowledge the incredible peers I had in our research group and those I had collaborated with, at USC and beyond. When I compile a research presentation or a paper, or this dissertation for that matter, I'm constantly reminded of their immense contribution in what I would present as my research results. And it's completely out of my imagination how things might have been, if any of them weren't there. Their collective contribution towards this dissertation is possibly way more than my own.

My earliest co-worker and partner in crime, Jubin Hazra, who introduced me to Professor Kapadia. It was from him that I learnt photolithography and metal evaporation, and general cleanroom use, as well as electronic device simulations. One of my earliest collaborators (from Professor Ravichandran's lab) and a very dear friend and someone I learnt a lot of theoretical and experimental aspects of materials science from – Dr. Shanyuan Niu – he's the one who helped me perfect my SEM skills, helped me understand the functioning and analysis of an XRD, and indirectly helped me mold my ways to be a better researcher. I had one of the most productive research comradeship with Wei Wang – the three papers I could write with her close contribution essentially created the basis of my Ph.D. work. I have always been inspired to make myself more organized and focused on work at hand, from Dr. Fatemeh Rezaeifar; and to be more professional,

from Dr. Qingfeng Lin. Jun Tao and Hyun Uk Chae are two of my close junior colleagues who have been very instrumental in the latter part of my Ph.D., and with whom I hope to publish a few more papers in the very near future. Several of my other junior colleagues have been very helpful in contributing to much of the heavy-lifting in different aspects of the workflow, and thereby allowing us to make progress as a team. Of them, Sizhe Weng, Yunpeng Xu, Dingzhu Yang, Chenhao Ren, Shreyas Naik, and Bamdad Mesri deserve special mention. Another person whom I've worked less on research but have talked the most on non-research stuff with (particularly on sociopolitical matters) is Ragib Ahsan. I continue to be inspired by his scientific mind during research group meetings, and our few scientific discussions in the office. A big thanks to Dr. Mitchell Dreiske for being a very helpful peer in several of the academic courses we took together, as well as for teaching me the details of the MOCVD reactor. Matthew Yeung and Louis Blankemeier are two of the most amazing undergrads I've had the opportunity to work with, during their times at USC and beyond.

I also owe my appreciation to Dr. Matthew Mecklenburg and Arashdeep Singh Thind (from Prof. Rohan Mishra's group at WUSTL) for their excellent STEM characterization of my samples, and to Dr. Andrew Clough for his thorough XPS analysis of my samples.

And of course, there are many more whom I may regard as my cleanroom buddies – Dr. Dongseok Kang (who taught me many useful cleanroom tricks), Huandong Chen, Yongkui Tang, Lurui Zhao; peers from Professor Cronin's lab which used to be my second most visited places after our own – Dr. Rohan Dhall, Dr. Haotian Shi, Dr. Bingya Hou, Dr. Nirakar Poudel, and so on; peers from Professor Ravichandran's lab – Mythili Surendran, Yang Liu, Thomas Orvis, Boyang Zhao; peers from Professor Madhukar's lab – Swarnabha Chattaraj and Lucas Jordao; peers from Professor Wang's lab – Huan Zhao and Xiaodong Yan; all of whom I have a very cordial relationship with.

I would also like to appreciate the help from our department's research administrators who play an immensely important role in keeping our research run smoothly – Kim Reid, Susan Zarate, Esrath Rumki, Diana Vuong, Jennifer Ramos, Sunny Bhalla, Kalief Washington, and Birgitte Hunt – I've worked with all of them at different times. Also thanks to Diane Demetras, Tracy Charles, Jennifer Gerson, and Kate Tegmeyer: all of whom have helped me through my Ph.D. as they help many others. Special shout-out to Cathy Huang and Ben Paul.

A very brief but vivid thanks to all my high school and undergraduate teachers and friends (many of whom are also currently pursuing or already finished their Ph.D.) – I'm blessed to have you in my network, and am constantly inspired by your achievements.

Finally, I would like to express my heartiest gratitude to my roots in India – my parents Debjani Sarkar and Basudeb Sarkar, my brother Deep Sarkar, my grandparents, my aunts, uncles and cousins, and everyone else who had helped me in reaching here, and who were constantly with me in their mind, spirit and prayers throughout my Ph.D. journey.

Abstract

Building Blocks for 3D Integrated Circuits: Single Crystal Compound Semiconductor Growth and Device Fabrication on Amorphous Substrates

by

Debarghya Sarkar

Committee: Prof. Rehan Kapadia (Chair), Prof. Michelle Povinelli, Prof. Jayakanth Ravichandran, Prof. Han Wang

Over the past five decades, the world has made rapid technological progress supported by the advancement in solid-state electronics and photonics. Referred to as the Moore's Law, the fundamental mechanism for making a better microprocessor chip has been the reduction of footprint of individual operational units (field effect transistors), thus increasing the chip functionality and performance by increasing planar density. However, there is an impending problem. Improving integrated circuits by device miniaturization is coming to an end, since device miniaturization is reaching its fundamental physical limit. A potential novel approach for continued improvement is a three dimensional (3D) multifunctional integrated circuit. However, there are several challenges associated with fabricating a 3D IC, and this dissertation is aimed at experimentally establishing the viability of potential solutions to some of the fundamental problems. Those are: (i) the ability to integrate single crystal semiconductors on an amorphous buffer, (ii) at a temperature below 400 ^{0}C so that underlying active layers are not affected, and (iii) to be able to fabricate high-performance devices out of them.

A recently introduced non-epitaxial growth technique called thin film – vapor liquid solid growth that showed the ability to grow large area grain size (10-100 μm) polycrystalline film on metal foils, has been adopted as the primary material growth method. It has been first generalized to be integrable on any substrate including amorphous and crystalline dielectrics (*i.e.* not just limited to metals), and its geometrical constraints from a thermodynamic perspective are established. This has allowed for a wide variety of compound semiconductor materials (III-Vs and IV-Vs) to be able to be grown as templates upto tens of micron in lateral dimension on a wide variety of technologically relevant substrates. Extensive photoluminescence measurements and analyses have been performed, which indicate excellent optoelectronic performance comparable to that of commercial single crystal InP wafer. Temperature dependent photoluminescence, Hall mobility, and electron back-scatter diffraction studies demonstrate the ability to grow high quality single crystal III-Vs below 400 ^{0}C on amorphous substrates including on flexible substrates such as polyimide. Room temperature Hall mobility reaching 6000 cm^2/V-s for InAs grown at 300 ^{0}C on HfO_2, and contact-resistance limited FET mobility of 500 cm^2/V-s for InP grown on SiO_2, have been shown: one of the highest values so far for any material family directly grown on an amorphous dielectric. A scalable platform for obtaining artificial synapses has been demonstrated by modulation of oxide-semiconductor interface trap occupancy in InP nanowire FETs. Finally, selective growth of MOCVD epitaxial layers on these single crystal templates have been briefly studied as precedents to obtain ultra-high performance devices on the back-end of CMOS chips.

Table of Contents

Chapter 1

A Brief Summary of my Research

My Ph.D. research has been centered on materials and device innovation as potential candidates for future three dimensional integrated circuits (3D ICs). This chapter of my dissertation highlights the main research results in a comprehensive but relatively high-level narrative. Following chapters build on the highlights mentioned here, and give an in-depth fine-detailed-technical description of the experiments and their outcomes.

1.1 3D Integrated Circuits: Why? What? How?

Let us start with the question: *why do we need 3D integrated circuits?*

Over the past five decades, the world has witnessed rapid technological growth driven by progress in computational ability. This increase in the operational bandwidth has been engineered by integrating a higher number of operational units per unit area of the microprocessor chip by reducing the size of each operational unit, called Field Effect Transistor devices (FETs). Famously referred to as the Moore's Law,[1] this trend of making a better microprocessor chip by incorporating larger number of FETs, has been successfully followed for multiple consecutive generations of chip design (Figure 1.1). However, there is an impending problem. Improving integrated circuits by device miniaturization is coming to an end, since device miniaturization is reaching its fundamental physical limit. A potential novel approach for continued improvement is a three dimensional (3D) multifunctional integrated circuit.

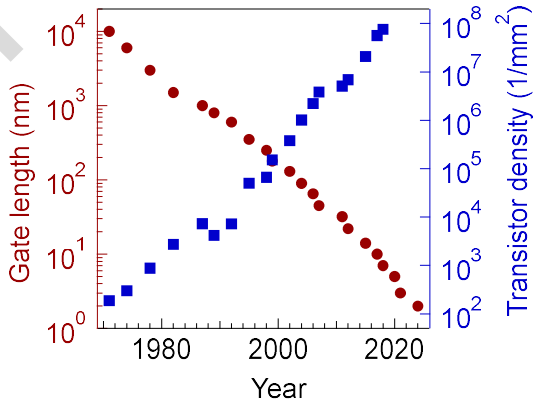

Figure 1.1: Historical trend of increasing device density and reducing device dimension. Data from en.wikipedia.org/wiki/Moore%27s_law and …/Transistor_count

What can be a zeroth order description of of a 3D IC architecture?

A representative cartoon of a 3D multifunctional integrated circuit is shown in Figure 1.2. Essentially, there would be multiple functional circuits for logic, communication, and memory operations stacked on top of each other in the same chip. One may think of it as a vertically stacked motherboard with different circuits performing modular functions (logic, memory, etc.) in the same chip, instead of different modular chips performing their functions and communicating across the present-day motherboard. It is important to have 3D to get higher density of integration (versus state-of-the-art 2D integration). And it is important to integrate multiple materials to achieve multiple functionalities, since each material is ideally suited for unique applications. Silicon has been the backbone material for the semiconductor industry all along due to early advantages in manufacturing processes. But it is far from being the ideal semiconductor material considering performance of devices. Compound semiconductors are a general class of materials that have electronic and optoelectronic properties far superseding that of silicon, but have not quite found their way into mainstream electronic devices because of economic disadvantage in traditional growth processes and difficulty in efficient integration.

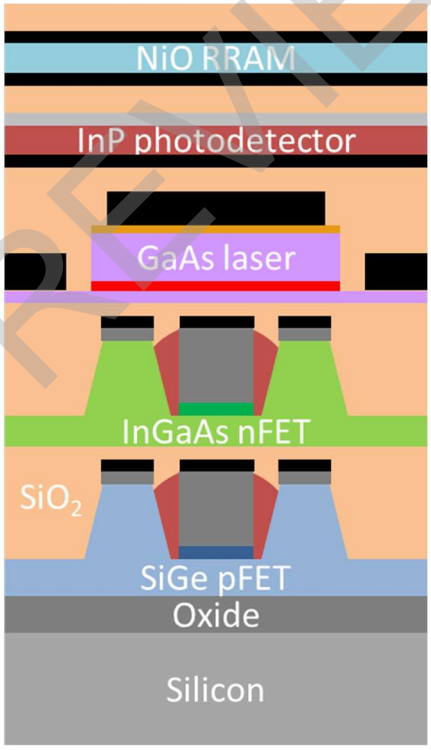

Figure 1.2: Schematic representation of a potential 3D IC stack.

So how can we fabricate such a structure?

There are several challenges associated with fabricating a 3D IC so that no commercial 3D IC exists today despite this idea being there for literally decades. This dissertation is aimed at solving some of the most fundamental problems to help pave the way forward. Those are:

(i) we need to integrate single crystal semiconductors on an amorphous buffer,
(ii) at a temperature below 400 ^{0}C so that underlying active layers are not affected, and
(iii) we should be able to fabricate high-performance devices out of them.

1.2 Epitaxial lift-off and transfer

The most widely used approach towards that currently followed, is some variant of this method called *epitaxial growth and transfer*.[2] In this case, semiconductor layers are epitaxially grown on lattice matched substrates, and through multiple steps, transferred to the host substrate on which devices are fabricated (Figure 1.3). This is successfully followed in many academic setups and in some commercial applications, but there are also some well-known important drawbacks: the process is expensive, is not scalable over large areas required for industrial production, and has access to limited materials stemming from lattice matching and suitable release-process constraints.

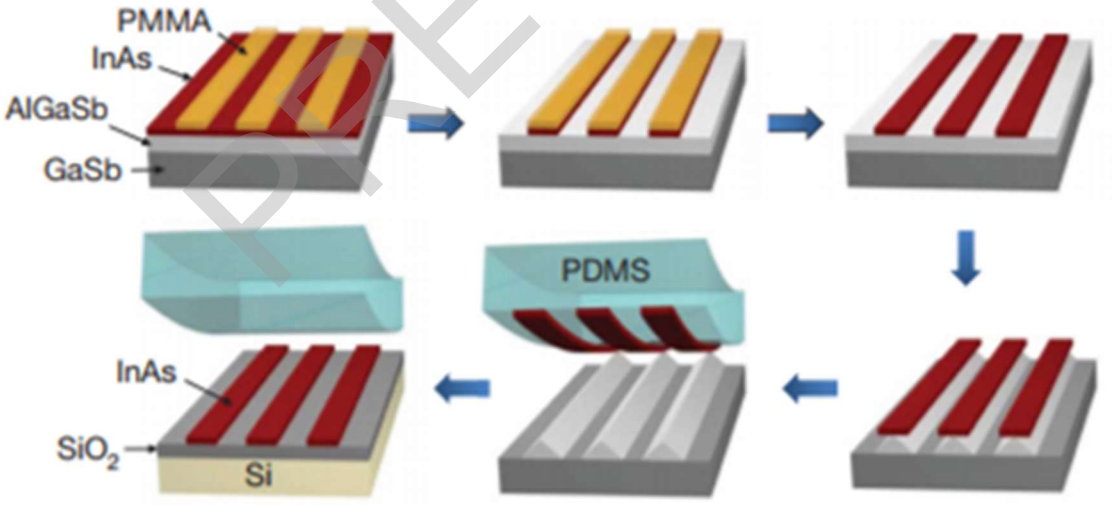

Figure 1.3: Integration of high performance devices by epitaxial lift-off and transfer. Reproduced with permission from [2]. Copyright 2010, Springer Nature.

1.3 Direct non-epitaxial growth?

Alternatively, can we directly grow single crystal materials on amorphous materials instead? The traditional methods for semiconductor growth such as *metal-organic chemical vapor deposition* (MOCVD) and *molecular beam epitaxy* (MBE) would give single-crystalline growth only when grown on single-crystal substrates. On the other hand, these methods would give a poly-crystalline material (Figure 1.4) when grown on a buffer layer which is inherently amorphous.[3] Poly-crystalline materials would give device performance that are orders of magnitude lower than that of their single-crystalline counterparts. This is the most important roadblock that has prevented efficient integration of multifunctional high-performance devices in the past.

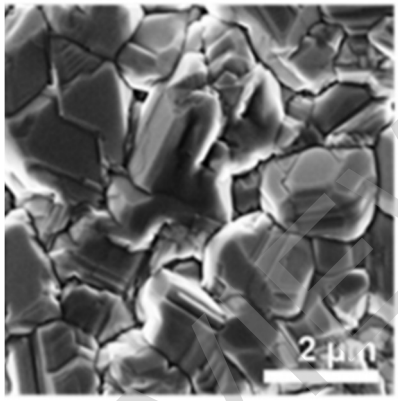

Figure 1.4: Polycrystalline InP by MOCVD directly on amorphous Mo foil. Reproduced with permission from [3]. Copyright 2012, American Institute of Physics.

1.4 Thin Film – Vapor Liquid Solid growth

On the other hand, a novel growth technique was recently developed, called thin film vapor-liquid-solid,[4, 5] where it was shown that large area single crystal indium phosphide (InP) with grain size of the order of 100 µm to 1 mm can be grown on refractory metal foils (Figure 1.5). This was the first step towards growth of crystalline compound semiconductor film on a non-epitaxial substrate.

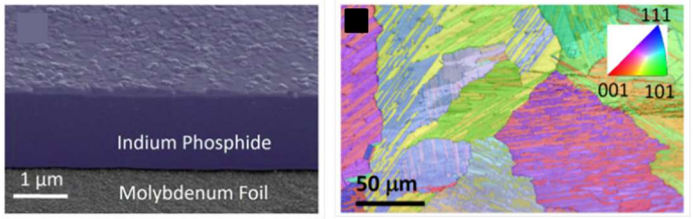

Figure 1.5: Ultra-large-grain size polycrystalline InP by TF-VLS directly on amorphous Mo foil. Reproduced with permission from [4]. Copyright 2013, Springer Nature.

How is it done? Well, as represented in Figure 1.6 (a), indium (In) is first deposited on molybdenum (Mo) foil, and capped with silicon dioxide (SiO_2). This is then taken to the furnace and heated to a growth temperature of 450-800 ^{0}C, where In is molten. Phosphorus (P) is introduced in the vapor phase which percolates through the SiO_2 capping layer, and gradually saturates liquid In. As it gets slightly supersaturated, InP is precipitated. Now, once the first InP nucleus forms, a depletion region of P is created around it driven by the high diffusivity of P in liquid In, such that the concentration of P in that region is always below the solubility of P in liquid In, and no InP is nucleated in this region. The second InP nucleus forms a distance away from the first, of the order of 100 µm to 1 mm, determined by the P flux and the initial In thickness.

The plot in Figure 1.6 (b) is an experimental verification of this model, where it is seen that the nucleation density reduces with lower P flux, thereby giving rise to larger grain sizes. This work was pioneered by Kapadia *et. al.* at UC Berkeley.

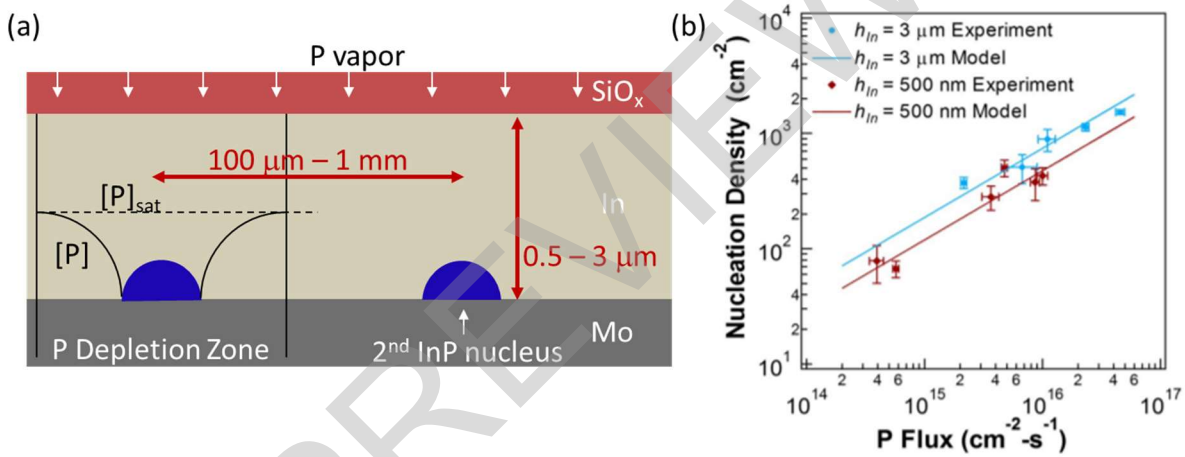

Figure 1.6: (a) Schematic of controlled grain size in TF-VLS growth. (b) Experimental verification of nucleation model. Reproduced with permission from [4]. Copyright 2013, Springer Nature.

1.5 *Templated* Liquid Phase (TLP) growth

Then it was proposed that if we pattern the indium so that the lateral dimension is less than a typical depletion length, each pattern will form only a single crystal.[6]

1.5.1 Single Crystal Compound Semiconductor mesas on Diverse Substrates

Building on that, my research efforts first demonstrated growth of single crystal compound semiconductor mesas on diverse substrates.[7]

Schematically shown in Figures 1.7 (a-d), we start with patterns of In capped with SiO_2 on a substrate. This is then taken to the growth furnace and heated to the growth temperature in presence of phosphine (PH_3). The PH_3 flux is controlled to ensure single nucleation in each pattern, which with time, gradually grows as a single crystal to achieve single crystal InP in each pattern. Figures 1.7 (e-h) are a sequence of SEM images of InP nucleating in a pool of In, gradually growing as a single crystal until the entire pattern is transformed to InP, so that the entire pattern is a single InP crystal (which in this case, is 6 µm diameter). Although InP is used to describe this process, it may be noted that it's not just InP that can be grown by this process. In fact we have grown many different materials, and on a wide variety of substrates, as shown in Table 1.1.

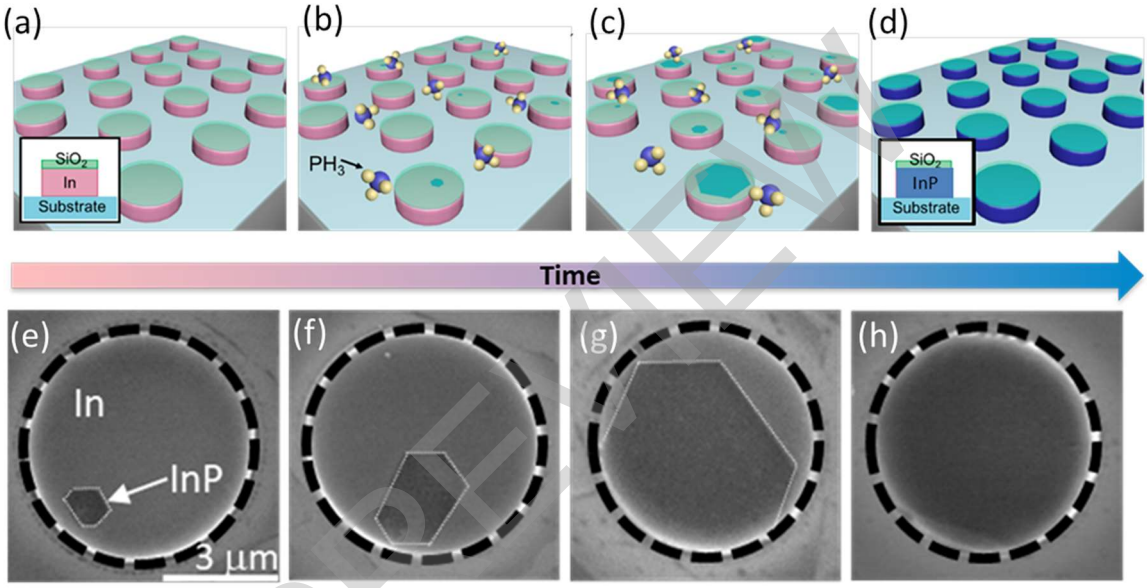

Figure 1.7: (a) Schematic of TLP growth of InP on any substrate. (b) Representative SEM of InP nucleating and growing in a pool of indium. Reproduced with permission from [7]. Copyright 2018, American Chemical Society.

Materials	**Substrates**
III-V binary: InP, GaP, InAs	Refractory Metals: Mo, W
III-V ternary: $In_xGa_{1-x}P$	Amorphous: MoO_x, SiO_2, Si_3N_4,
IV-V binary: SnP, Sn_4P_3	Al_2O_3, TiO_2, ZrO_2, HfO_2
Heterojunction: InP/Sn_4P_3	Crystalline: Gd_2O_3, Er_2O_3, $SrTiO_3$
	2-D: Graphene
	Polymer: Polyimide

Table 1.1: Different materials grown by TLP method on different substrates.

As representative examples, Figures 1.8 (a-c) are some experimental results, showing growth of different stoichiometries of indium gallium phosphide, different stoichiometries of tin phosphide, as well as an atomically sharp lateral heterojunction between InP and Sn_4P_3.

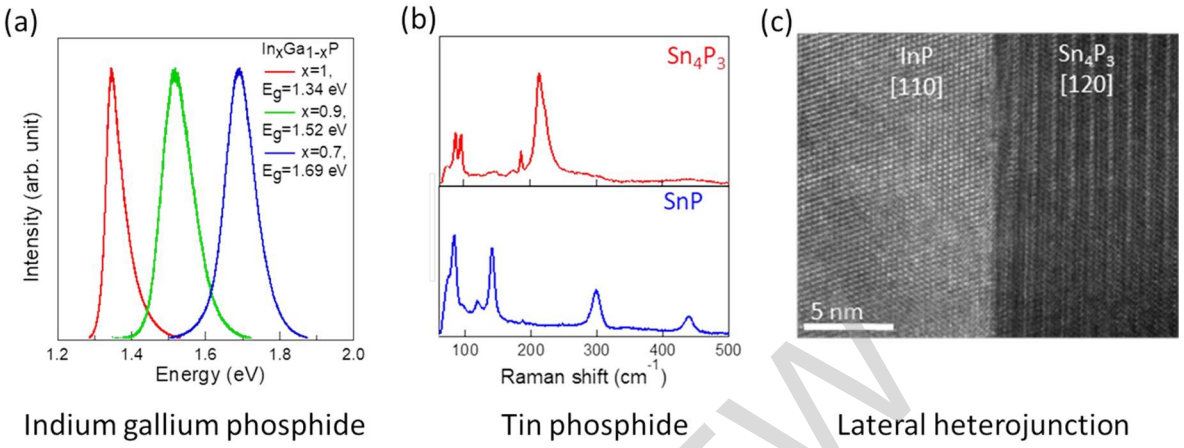

Figure 1.8: (a) In-Ga-P, (b) Sn-P, (c) InP-Sn_4P_3 lateral heterojunction grown by TLP method. Reproduced with permission from [7]. Copyright 2018, American Chemical Society.

Also, Figures 1.9 (a-c) are transmission electron microscope images showing InP grown on crystalline Gd_2O_3, amorphous TiO_2, and 2D graphene.

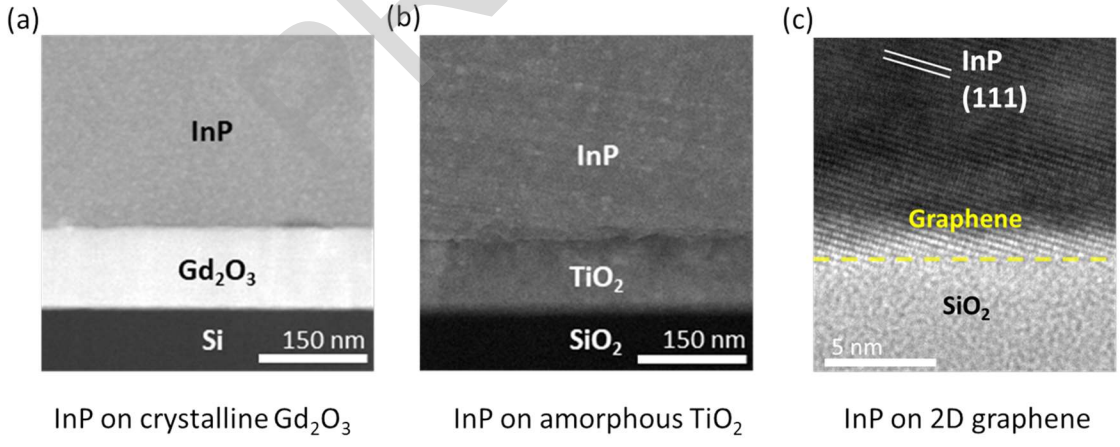

Figure 1.9: InP grown on (a) crystalline Gd_2O_3, (b) amorphous TiO_2, (c) 2D graphene. Reproduced with permission from [7] (Copyright 2018, American Chemical Society) and [9] (Copyright 2018, American Vacuum Society)

1.5.3 Large Area (>100 μm) Single Crystal

Moving forward, we worked on expanding the area of the crystal, *e.g.* the mesas in Figure 1.10 (a) are over 100 μm in length and 5 μm in width. As evident by electron backscatter diffraction (EBSD) inverse pole figure imaging in Figure 1.10 (b) (i-vi), each mesa is represented by a single color, and is therefore a single crystal.

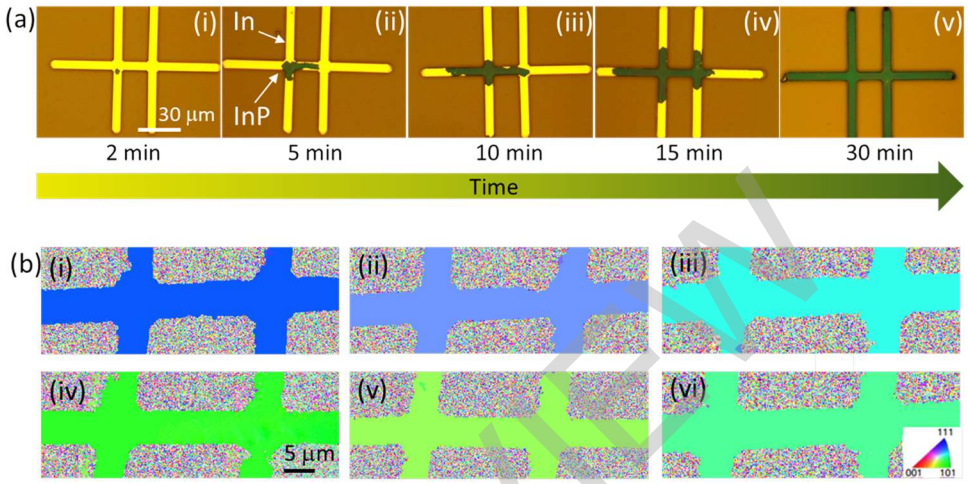

Figure 1.10: (a) InP growing as a single crystal in a Hall element structure, (b) single crystallinity indicated by EBSD.

1.5.4 Crystal Quality Analysis of TLP InP

Figure 1.11 is a collage of representative (scanning) transmission electron microscopy (S)TEM images of TLP InP. Figure 1.11 (a) shows InP growing directly on graphene transferred on SiO_2. The selective area electron diffraction (SAED) in Figure 1.11 (b) and the high resolution TEM in Figure 1.11 (c) indicate the high crystalline quality of the grown films. However, it may also be noted that given the stacking fault energy for III-Vs is low, these grown films often have multiple stacking faults as shown in Figure 1.11 (d) and twinning present within the crystals as in Figure 1.11 (e).

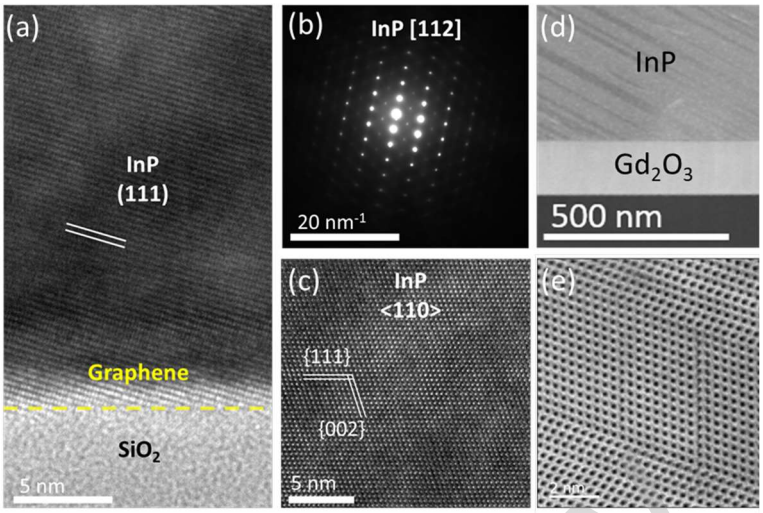

Figure 1.11: (a) STEM image of InP on graphene transferred to SiO_2, (b) SAED and (c) STEM image of InP on TiO_2, (d) Stacking faults in InP on Gd_2O_3, (e) Twinning in InP on HfO_2.

1.5.4 Surface roughness of TLP materials

As seen in Figure 1.12, the typical surface roughness of the grown films can be controlled to within 1-2 nm RMS roughness. This is mainly determined by the initial indium film roughness, which is controlled by evaporating indium at relatively low rates and with the samples connected to a liquid nitrogen cooled stage to reduce surface mobility of incident In atoms.

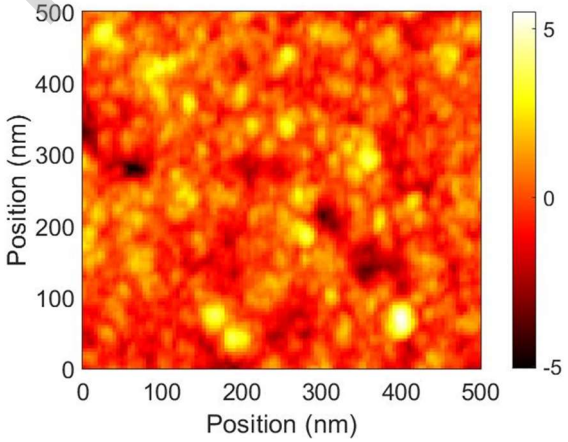

Figure 1.12: AFM map of representative TLP InP surface.

1.5.5 Dewetting of Liquid Indium on Diverse Substrates

Before we go forward, it may be better to take a step back and recognize that the translation from growth on metals to growth on dielectrics is actually non-trivial. Compared to this flat film of InP on Mo (Figure 1.13 (a)), when similarly tried to be grown on SiO_2 (Figure 1.13 (b)), it doesn't stay flat. When patterned on molybdenum oxide (MoO_x), it stays as intended (Figure 1.13 (c)), but forms holes when done on dielectric surfaces (Figure 1.13 (d)). The reason is that most substrates are "indium-phobic" causing In to dewet when it's molten.

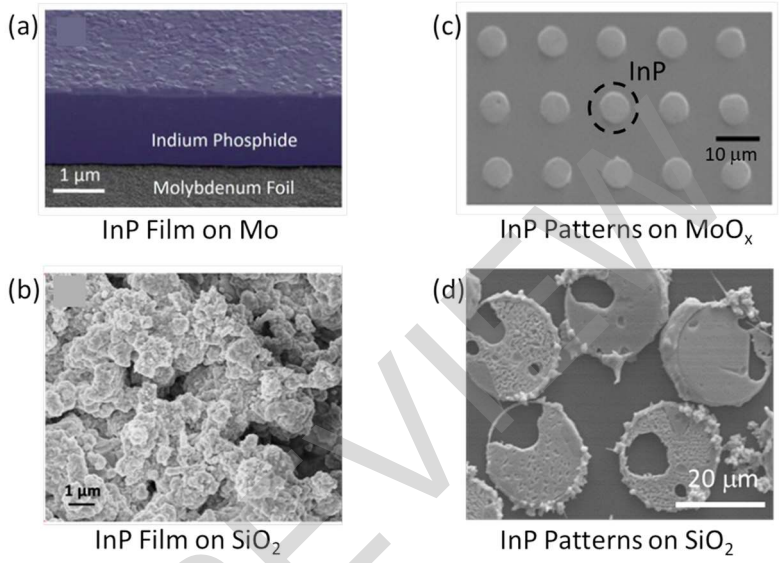

Figure 1.13: Representative InP growth on different substrates before wetting control.

To understand this better, we worked on a thermodynamic model, where we calculated the Gibbs free energy of formation of two different structures: one wetting *i.e.* without void (Figure 1.14 (a)), and one dewetting, *i.e.* with void (Figure 1.14 (b)). When we subtract one from the other, we get the Gibbs free energy of formation of the void, and plot it as a function of void radius (r) for different template radii (R_T). As can be seen here (Figure 1.14 (c)), that for a given initial thickness of In (h), there is finite probability of void formation, and a thermodynamically stable size of voids. On the other hand, no stable void formation would occur for templates below a certain size for the given indium thickness. In other words, liquid templates would always wet a given substrate once they are above a critical aspect ratio.