

Phase Control of RF Sputtered SnS_x with Post-Deposition Annealing for a Pseudo-Homojunction Photovoltaic Device

J.R. NASR,^{1,3} J.J. CORDELL,² R.L. GURUNATHAN,² J.R.S. BROWNSON,²
and M.W. HORN^{1,2}

1.—Engineering Science and Department, The Pennsylvania State University, University Park, PA 16802, USA. 2.—Materials Science and Engineering Department, The Pennsylvania State University, University Park, PA 16802, USA. 3.—e-mail: joseph.nasr7@gmail.com

Tin (II) Monosulfide (SnS) is an interesting material for thin film photovoltaics. *n*- and *p*-type sputter-deposited SnS_x have been investigated for use in a homojunction photovoltaic device. Post-deposition vacuum heat treatment of as-deposited amorphous films was found to produce *n*-type SnS_x and *p*-type SnS depending upon in situ vacuum anneal time and temperature. Annealing temperatures varied from 300°C to 400°C at durations from 20 min to 60 min under high vacuum. Results show clear photoresponse for both *n*-type and *p*-type using Pd contacts.

Key words: Solar cells, SnS, electronic, materials, absorber, thin film, sputtering

INTRODUCTION

In the quest to turn light into electricity, various types of solar cells have been suggested and developed: (1) inorganic solar cells incorporating semiconductor materials and next generation thin film solar cells, (2) dye-sensitized solar cells (DSSCs) consisting of light-absorbing dye molecules, oxidized semiconductor material, redox electrolyte, and catalyzed counter electrodes, and (3) organic solar cells with light-absorbing polymers and conductive polymers. Solar cells with thin film absorber layers, have been produced using cadmium telluride (CdTe), copper indium gallium selenide CuIn_xGa_{1-x}Se₂ (CIGS), and silicon (Si). Semiconductors materials incorporating IV-VI elements such as PbS, PbSe, and SnS possess excellent optical properties, in particular for the infrared (IR) region of the electromagnetic spectrum. Additionally, these semiconductors possess bandgaps that facilitate their application to near-IR or IR devices such as solar cells and infrared detectors.

SnS-based solar cells have the potential to achieve 24% efficiencies based on the optoelectronic properties of SnS_x,^{1,2} however, the best reported

device using SnS_x has produced less than 5% efficiency.³ SnS is a semiconductor material with reported direct and indirect band gaps of 1.33–1.55 eV^{4–6} and 1.07–1.39 eV,^{7–9} respectively. It has a high absorption coefficient of $>10^4$ cm⁻¹ and possesses other ideal physical properties; it is cost efficient, non-toxic, and abundant in the earth's crust. In addition, it possesses a high carrier concentration around 10^{17} – 10^{18} cm⁻³.¹⁰

For practical and economical solar cells, scientists and engineers rely on the use of thin film technology because it reduces the amount of active material in a cell. Several thin film fabrication methods for producing these films have been reported.¹¹ Many SnS synthesis studies have focused on low-temperature processing techniques, which result in complete sulfur use.^{12–15} However, wet chemistry techniques are not favorable for large-scale manufacturing of photovoltaic (PV) modules. Sputter deposition is known to produce high-quality films and is easily scalable. With the help of the plasma, extra energy is provided to the deposition precursors, which offers more film-growth control than non-plasma-based methods such as spray deposition. Even though the sulfur vacancies help to make SnS intrinsically *p*-type, defects can have deleterious effects on the electronic properties of the film. In

order to decrease the number of sulfur vacancies,⁶ a disulfide target was investigated as a way to increase the as-deposited sulfur content. Previous work from our group has shown that material properties such as film structure, resistivity, and absorption of films deposited using radio frequency (RF) magnetron sputtering vary with processing pressure, power, and throw distance.^{6,16} Only a few studies have investigated sputtered SnS_x, and none have fully explored the parameters available for fabricating and treating films.

The literature suggests that the use of proper top or bottom contacts and a matching heterostructure material such as CdS, could increase the efficiency of the device to approximately 10%.¹⁷ We have investigated bottom contact materials such as Pd for ohmic contacts with SnS. Initially, two optimal pathways were investigated for obtaining an *n*-type as well as a *p*-type SnS material by adjusting annealing conditions with the intent of evaluating a pseudo-homojunction photovoltaic solar cell.

METHODS AND MATERIALS

The depositions were made using a radio frequency (13.56 MHz) magnetron sputtering system oriented in a downward vertical geometry. The chamber was roughed to $\sim 6.66 \times 10^{-3}$ kPa and then pumped down with a turbomolecular pump to $< 2.66 \times 10^{-7}$ kPa. In order to minimize film contamination (mostly oxygen), depositions were spaced at least 12 h apart. A mass flow controller (MKS Instruments Model 247C 4-Channel) maintained argon gas flow of 40 sccm during deposition. The argon plasma was ignited using an Advanced Energy RFX-600 as the RF power supply coupled with an impedance matching network (Advanced Energy Model ATN 500). Plasma was ignited at pressures in the range of 7.99×10^{-3} – 9.33×10^{-3} kPa and then was reduced to the desired pressure. Depositions were carried out using a 3" diameter, 0.125" thick tin disulfide target of 99.999% purity manufactured by LTS Research Laboratories.

Pathways were investigated for obtaining *n*-type and *p*-type SnS material by adjusting annealing conditions with the hope of fabricating a SnS-pseudo-homojunction-based photovoltaic solar cell. Depositions were conducted at a fixed power (115 W), pressure (1.3^{-3} kPa), and time (10 min) on silicon–nitride–coated silicon wafers and glass microscope slides. A series of anneals using a lamp heater under vacuum ($\times 10^{-7}$ kPa) were executed at temperatures of 300°C, 400°C, and 425°C, lasting from 20 min, 30 min, and 60 min. Usually, the ramp time to reach the desirable temperature was around 5–7 min. After the annealing time elapsed, the chamber was backfilled with N₂ to accelerate cooling. It took approximately 30 min to cool to 50°C (as shown in Fig. 1) for the 400°C for 60 min anneal (P1). Silicon and glass substrates were used with Pd bottom contacts. All deposition conditions for

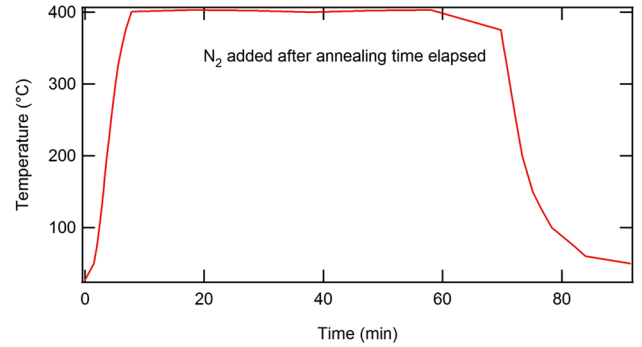


Fig. 1. Temperature (°C) versus time (min) ramp-up/annealing time/ramp-down for a 400°C for 60 min anneal (P1).

amorphous, *p*-type, and *n*-type materials are shown in Table I. The anneal temperatures and times in Table I do not include the ramp-up/ramp-down times. To ensure reproducibility, a timer was set for the giving annealing time when the temperature reached the desired. The offset at 40 min shows that the temperature went slightly below 400°C. Figure 2a and b show a schematic picture of both film stacks, *p*-type and *n*-type, respectively, used in this investigation. Both pathways come from annealing an amorphous phase which is deposited at 115 W, 1.3^{-3} kPa for 10 min.

Since the goal was to deposit a pseudo-homojunction device in the same chamber without breaking vacuum, depositing a second film and annealing it on top of the *p*-type layer will result in annealing the bottom film longer than previously optimized. In order to verify the *p*-type layer did not experience any negative alterations during the second deposition and anneal (*n*-type), we evaluated a double-annealed *p*-type layer.

The first sample had an anneal at 400°C for 60 min (*p*-type) followed by an anneal at 400°C for 20 min (D1). The second sample had an anneal at 400°C for 60 min followed by an anneal at 300°C for 20 min (D2). Lastly, since the results obtained did not satisfy the needs of the device and the *p*-type layered was altered, the annealing temperature of the *p*-type layer was increased from 400°C to 425°C and this sample was further annealed at 400°C for 20 min shown in Table I. For samples D1, D2, and D3 both annealing temperatures and times are shown.

Film Thickness and Deposition Rate

Before proceeding with the film deposition, the silicon–nitride–coated silicon wafers of about 1.5×1.5 cm² were painted with a thin strip of colloidal graphite. Colloidal graphite does not interact with the SnS deposited. After completion of the deposition, the deposited wafers are then placed in an ultrasonic acetone bath for 1–5 min, on average, to remove the colloidal graphite. The acetone liquid was replaced after every two baths. These baths

Table I. Summary of deposition parameters and annealing conditions

Sample name	Annealing temp. (°C)	Time (min)	Thickness (nm)	Deposition rate (Å/s)
A1	N/A	N/A	215.65	4.49
P1	400	60	259.65	4.43
N1	400	30	202.1	3.37
N2	300	20	275.63	4.59
N3	400	20	270.4	4.51
N4	300	30	247.3	4.12
P2	425	60	260.9	4.33
D1	400/400	60/20	263.5	4.39
D2	400/300	60/20	260.6	4.34
D3	425/400	60/20	260.15	4.33

Samples D1, D2, and D3 are double-anneals. The annealing conditions shown are for both anneals. The first anneal for these three samples are 400°C for 60 min.

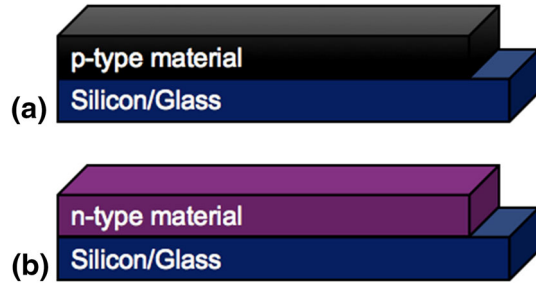


Fig. 2. (a) Silicon and glass substrates with a SnS_x *p*-type layer material. Similarly, (b) silicon and glass substrates with a SnS_x *n*-type layered material.

were constantly monitored in order to achieve complete removal of the colloidal graphite without damaging the film. Soon after the graphite was removed, the wafers were washed with isopropyl alcohol (IPA) and immediately blown dry with N₂ gas. A KLA-Tencor 500 Alphastep stylus surface profilometer (vertical resolution of 5 Å) was used to measure the step height from the film to the bare wafer surface. In order to obtain a good average thickness, three profilometer measurements were taken on five different spots for accuracy. The average thickness was then divided by the time to determine the average deposition rate.

Crystal Structure

The crystal structure was analyzed using glancing incidence x-ray diffraction (GIXRD) measurements on the glass substrates. The x-ray diffraction measurements were performed using the PANalytic X'Pert Pro MPD at an incidence angle of 1° while detecting at angles between 20° and 45°. 2 theta was plotted versus intensity and compared to standard reference peaks.

Electrical Properties

A Ti/Pd transmission line measurement (TLM) rectangular structure was deposited by e-beam

evaporation through a stencil mask at a deposition rate of 1 Å/s onto the SiN substrates. The SnS thin films were then deposited on top of the TLM bottom contacts in order to measure resistivity. Contact studies in our group determined that a higher work function metal like palladium (5.2–5.6 eV) could decrease the contact resistance to the SnS films and make a good ohmic contact unlike Al, Mo, or Ti. Since Pd can have adhesion problems, a 5 nm Ti layer was deposited before the 100 nm Pd was deposited. The contact spacing (d) from left to right are $d_1 = 0.02$ cm, $d_2 = 0.03$ cm, $d_3 = 0.05$ cm, and $d_4 = 0.07$ cm as shown in Fig. 3. The contact length (Z) is constant in all contacts. The resistance (R) from each film was plotted against the spacing to extract sheet resistance (R_{sh}) using the relationship below:

$$R_{sh} = \text{slope} \left(\frac{R}{\text{spacing}} \right) \times Z \quad (1)$$

The contact length was 0.6 cm for bottom contacts. Resistivity (ρ) was calculated using (2) as a function of the thickness (t):

$$\rho = (R_{sh}) \times t \quad (2)$$

The current–voltage (I-V) measurements were performed on a Wentworth Laboratories probe station connected to an Agilent HP 4156B Precision Semiconductor Parameter Analyzer. The samples were illuminated with a light emitting diode (LED) flashlight in the probe station to measure light I-V curves. Resistivity measurements were also taken on silicon and glass substrates (no TLM contact) using a four-point probe to compare results.

Conductivity

Samples were determined to be *n*- or *p*-type, using the hot point probe technique.¹⁸ This technique involves the heating one of the positive probe of a voltmeter to create a voltage over two points on the sample. A positive reading indicated *n*-type, and a negative reading indicated *p*-type.

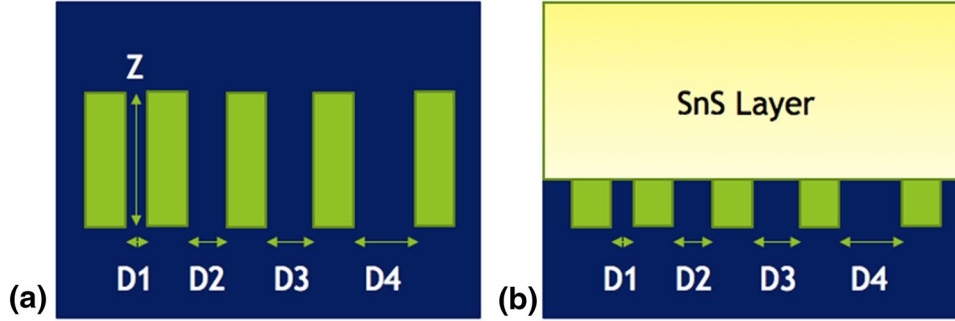


Fig. 3. Transition line measurement (TLM) bottom contacts on a silicon substrate. (a) 100 nm Pd TLM rectangular contact on top of the silicon-nitride-coated silicon. (b) The SnS layer is deposited on top of the contacts. By using an upside down silicon substrate a certain area of the film is protected to be enable measurement.

Optical Properties

Transmittance and reflectance spectra were measured for the SnS-coated glass slides about $1 \times 1 \text{ in}^2$ by using a Perkin Elmer Lambda 950 spectrophotometer over a spectral range from 300 nm to 2000 nm.¹⁹ Band gaps are determined through the methods outlined by Pankove.²⁰ However, as the films have non-negligible reflectance for the range of analysis, the required relationship to approximate α (absorption coefficient) for films with high reflectance in the range of analysis, must be determined by the equation below.

$$\alpha = -\frac{1}{d} \ln \left(\frac{T}{1-R} \right). \quad (3)$$

RESULTS AND DISCUSSION

The SnS thin films in this study were characterized for structure, optical absorption, and electrical properties. Table II shows the annealing parameters for ten different samples as well as their associated electrical properties.

Thickness

Post deposition annealing showed that heating temperature variations from 300°C to 425°C at a constant pressure of 1.3^{-3} kPa did not have much impact on the film thickness of the samples. Note that the thicknesses in Table I were measured after annealing. Neither double-anneal samples experienced much change in thickness. The thin films, sputtered from the SnS₂ target, were typically deposited more than twice as fast as the thin films that were sputtered from the SnS target.^{6,18}

Crystal Structure

Sputtering from a SnS₂ target produces sulfur-rich tin sulfide thin films, which can be annealed to produce various tin sulfide phases depending on anneal temperatures and time. The higher vapor pressure of S over Sn results in higher Sn content in

SnS_x films with heating depending on the temperature, duration, and gas overpressure during the anneal. These annealing conditions can be tuned to obtain specific phases and mixtures of phases in SnS_x resulting in different properties as highlighted in this section and the following segment on electrical and optoelectronic properties. Samples showed different structures including: Herzenbergite SnS, Berndite-2T SnS₂ and Ottomannite Sn₂S₃. In this annealing study, only SnS and Sn₂S₃ were obtained. XRD of these phases is shown in Fig. 4, while more extensive investigation of these phases and of SnS₂ can be found in previous literature from this research group.^{18,21} As-deposited SnS showed to be amorphous. The SnS phase obtained by annealing at 400°C and 425°C for 60 min displayed strong *p*-type behavior. Mixed phases resulted in *n*-type conductivity or no conductivity. Double-anneal D1 and D2 showed a change in crystal structure. After annealing both *p*-type layers, the film no longer had the monosulfide layer. Nevertheless, after annealing the *p*-type at a higher temperature followed by annealing a second time, the film remained in the Herzenbergite phase as shown in Fig. 5.

Electrical and Optoelectronic Properties

Resistivity was also measured using a four-point probe. As-deposited SnS on glass showed lower resistivity, by several orders of magnitude, than that deposited on silicon. We attribute this to the difference in thermal and electrical conductivity of the substrates. The lowest resistivity value obtained on 4-point probe measurements, 23.64 Ω-cm, was for *p*-type SnS (P1) on glass.

Palladium bottom contacts were deposited on SnS_x layers on silicon substrates. TLM measurements of these films showed that films deposited at room temperature and subsequently annealed have lower resistivity than films not annealed. These resistivities of 1–150 Ω-cm are close to the reported resistivity of polycrystalline SnS. An increase in temperature and time of anneals decreased resistivity significantly. Annealed samples also had

Table II. Resistivity for films determined by TLM measurements with Pd bottom contacts on Si substrates and four-point probe

Sample name	Resistivity from 4 pp on silicon (Ω-cm)	Resistivity from 4 pp on glass (Ω-cm)	Resistivity from TLM dark I-V (Ω-cm)	Resistivity from TLM light I-V (Ω-cm)	Conductivity type on silicon	Conductivity type on glass
A1	–	–	Not meas.	Not meas.	N/A	N/A
P1	64.45	23.64	46.93	39.56	<i>p</i> -type	<i>p</i> -type
N1	501.81	34.92	103.69	87.67	<i>n</i> -type	<i>p</i> -type
N2	–	–	Schottky	Schottky	N/A	<i>n</i> -type
N3	2561.9	226.61	164.89	105.36	<i>n</i> -type	<i>p</i> -type
N4	–	–	Schottky	Schottky	N/A	N/A
P2	205.64	83.91	Not meas.	Not meas.	<i>p</i> -type	<i>p</i> -type

Not meas. Resistivity was too high to measure.

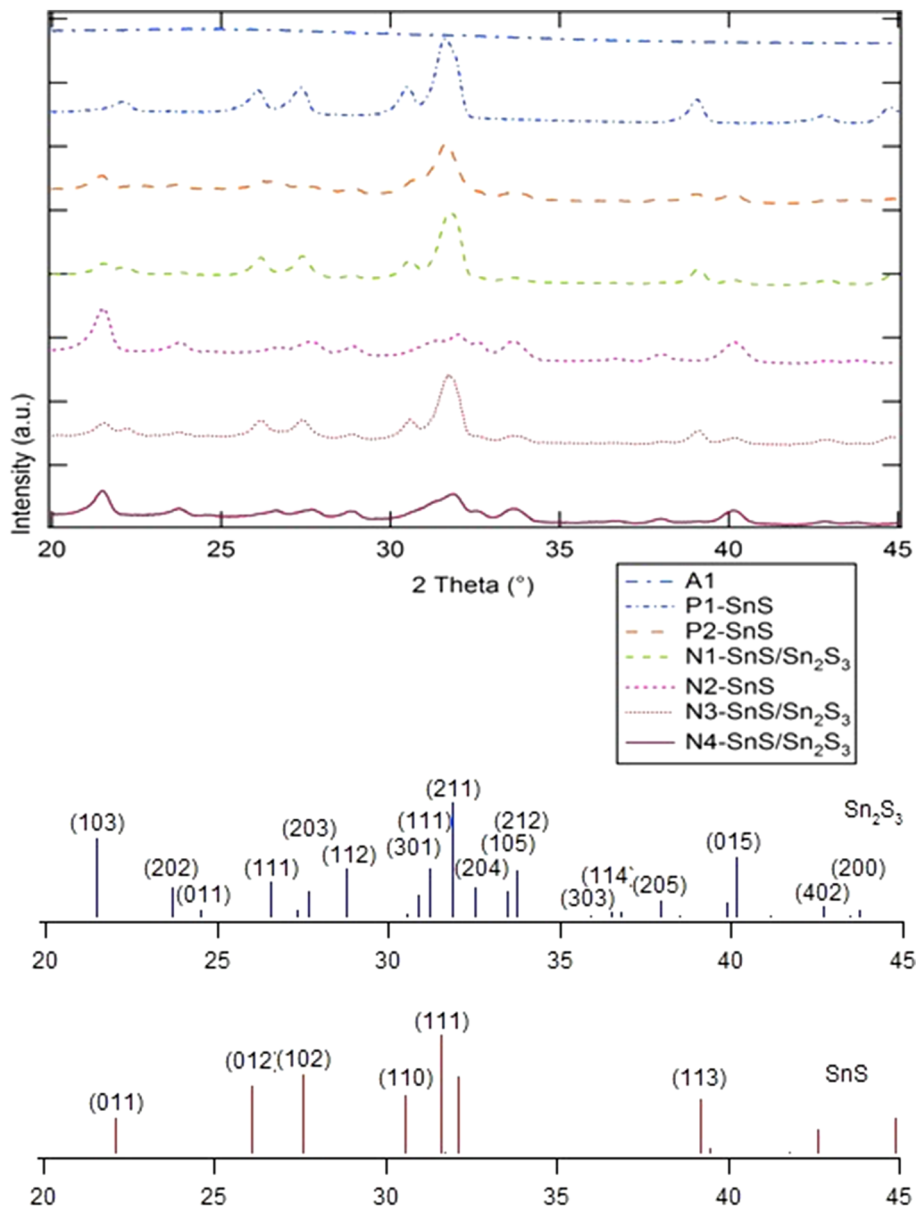


Fig. 4. XRD data for *n*-type and *p*-type films where annealing resulted in films with Sn₂S₃ and/or SnS phases are present.

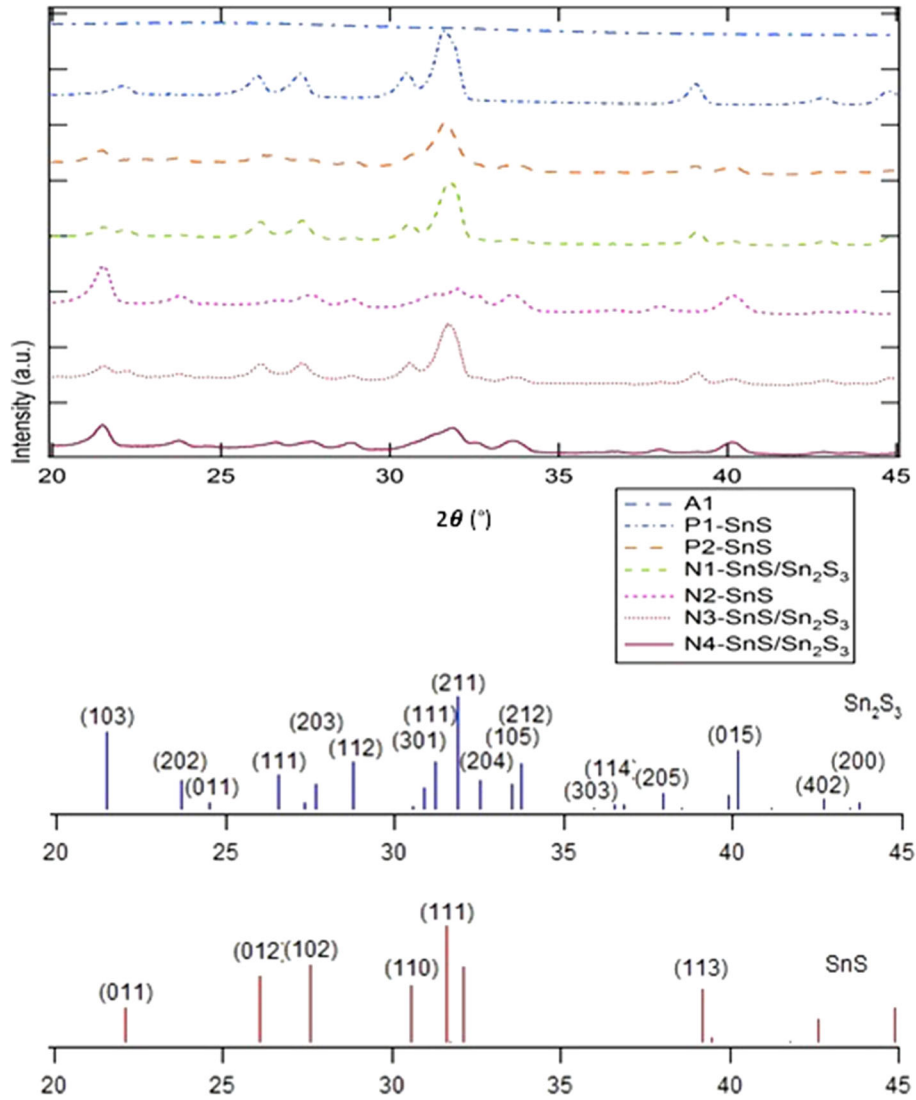


Fig. 5. XRD data for double-anneal films. D1 and D2 resulted in a mixed Sn₂S₃/SnS phase. D3 resulted in the SnS expected phase.

higher resistivity than samples deposited at elevated temperatures.²¹ Figure 6 shows that the metal–semiconductor interface has an ohmic contact. Sample P1 shows a dark 46.93 Ω -cm and light 39.56 Ω -cm. *n*-type films exhibits schottky behavior as expected, since Pd makes ohmic contact with *p*-type semiconductor. On the other hand, as expected, *p*-type SnS_x shows a low resistivity and linear I-V. Photoresponse was noticed by a decrease in resistivity when light was impinging from the top as shown in Table II. When measuring the conductivity of the films, the sign of the voltage drop detected indicated the carrier type.²² Since glass has a lower thermal conduction than silicon, SnS_x films did not get annealed at the same temperature as the silicon since the heating is in situ and in low vacuum and this the difference in conduction through the substrate likely influences the annealing temperature of the film on top.

The absorption coefficient of films, calculated from UV–Vis spectrophotometry data can be seen to onset at lower energy for the single phase, *p*-type SnS, sample P1 in Fig. 7. The *n*-type mixed phase film, N3, had comparable absorption coefficient, but onset at a higher energy while the amorphous film, A1 absorbed light to a lesser extent and onset slowly at energies greater than 1.5 eV in contrast to the steep slopes of the other films at this energy level. The absorption coefficients plotted exceed 10^5 cm⁻¹ and are slightly higher than those provided in the literature for sputtered SnS, which vary mostly from 10^4 cm⁻¹ to 10^5 cm⁻¹.¹⁸ The extracted band gaps for A1, P1, P2, N2, and N3 respectively, estimated by extending the slope of the absorption coefficient at onset are 1.7 eV, 1.3 eV, 1.4 eV, 1.8 eV, and 1.6 eV. These values correspond to direct band gaps of those materials although SnS is reported to have both a direct band gap at 1.8 eV

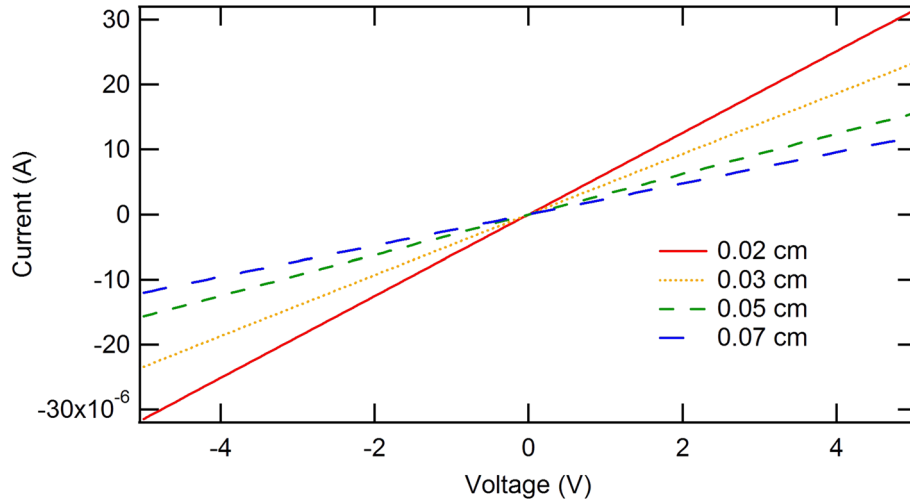


Fig. 6. TLM dark I-V curve on P1. Distances shown refer to the TLM contact spacing. The slope yields a consistent resistivity of 46.93 Ω -cm.

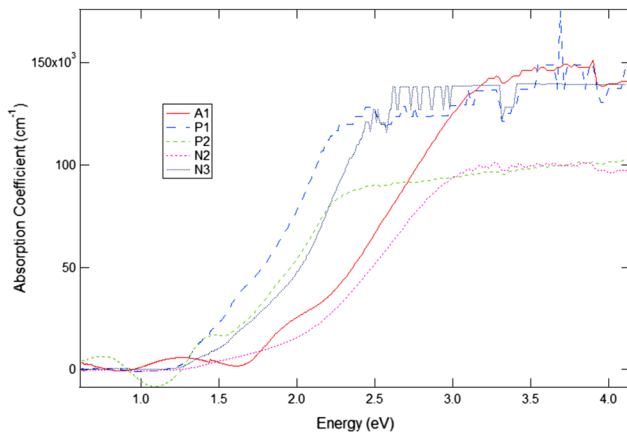


Fig. 7. Absorption coefficients of a *p*-type (P1 & P2), *n*-type (N2 & N3), and amorphous (A1) sample with respect to energy of incident light.

and an indirect band gap at 1.6 eV.¹⁸ The materials annealed for shorter periods of time or not at all, N2, N3, and A1 had higher band gaps than P1 and P2, which were annealed for three times as long as N2 and N3.

CONCLUSION

The films explored in this investigation yielded polycrystalline films of SnS and Sn₂S₃, as seen in the GIXRD data. The SnS phase was obtained by annealing at 400°C and 425°C for 60 min and displayed strong *p*-type behavior. Lower annealing temperatures resulted in *n*-type conductivity or low conductivity and were of mixed phase. Sputtering from the SnS₂ target deposits more than twice as fast as the films sputtered from the SnS target and results in the as-deposited amorphous film having the excess sulfur necessary to enable monosulfide formation during post-deposition annealing. The films showed some photoconductive response when illuminated by LED

flashlight. Two different methods were used to extract the resistivity of the sputtered SnS_x films. Four-point probe on SnS_x on glass and silicon substrates showed values as low as 23.94 Ω -cm. Rectangular palladium TLM bottom contacts were ohmic on *p*-type material and used to obtain dark and light resistivity as low as 46.93 Ω -cm and 39.56 Ω -cm, respectively. The films used in this study show a high absorption profile. The calculated absorption coefficients exceed 10⁵ cm⁻¹ and are slightly higher than those provided in the literature for sputtered SnS, which vary mostly from 10⁴ cm⁻¹ to 10⁵ cm⁻¹. The measured band gap falls into the optimal range for materials used in solar cells. The final resistivities of these samples are of the right magnitude for potential use in a pseudo-homojunction; however, more investigations are necessary to optimize this material and device structure, including the interface of the *n*-type and *p*-type material.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the assistance of the Materials Characterization Lab staff and facilities at Penn State University (UV-Vis and XRD). Additional thanks are extended to Drs. T. Jackson and S. Mohny and their students for allowing us to use their facilities for Pd depositions and electrical measurements.

REFERENCES

1. J.L. Loferski, *J. Appl. Phys.* 27, 7 (1956).
2. R. Chandrasakharan (Ph.D. dissertation, The Pennsylvania State University, University Park, PA, 2012).
3. P. Sinsermsuksakul, L. Sun, S. Lee, H. Park, S. Kim, C. Yang, and R. Gordon, *Adv. Eng. Mater.* 4, 15 (2014).
4. D. Avellaneda, M.T.S. Nair, and P.K. Nair, *J. Electrochem. Soc.* 155, 7 (2008).
5. F. Jiang, H. Shen, W. Wang, and L. Zhang, *J. Electrochem. Soc.* 159, 3 (2012).
6. R.E. Banai, H. Lee, M.A. Motyka, R. Chandrasekharan, N.J. Podraza, J.R.S. Brownson, and M.W. Horn, *IEEE J. Photovolt.* 3, 3 (2013).

7. S.S. Hedge, A.G. Kunjomana, K.A. Chandrasekharan, K. Ramesh, and M. Prashantha, *Phys. B* 406, 5 (2011).
8. T. Sorgenfrei, F. Hofherr, T. Jau[sz], and A. Croll, *Cryst. Res. Technol.* 48, 4 (2013).
9. W. Albers, C. Haas, and F. van der Maesen, *J. Phys. Chem.* 15, 3 (1960).
10. A.P. Lambros, D. Geraleas, and N.A. Economou, *J. Phys. Chem. Solids* 35, 4 (1974).
11. J.A. Andrade-Arvizu, M. Courel-Piedrahita, and O. Vigil-Galán, *J. Mater. Sci. Mater. Electron.* 26, 7 (2015).
12. J.R.S. Brownson, C. Georges, G. Larramona, A. Jacob, B. Delatouche, and C. Lévy-Clément, *J. Electrochem. Soc.* 155, 1 (2008).
13. M.M. Kamel, and M.M. Ibrahim, *J. Solid State Electrochem.* 15, 4 (2011).
14. K. Hartman, J.L. Johnson, M.I. Bertoni, D. Recht, M.J. Aziz, M.A. Scarpulla, and T. Buonassisi, *Thin Solid Films* 519, 21 (2011).
15. R.E. Banai, M.W. Horn, and J.R.S. Brownson, *Sol. Energy Mater. Sol. Cells* 150, 112 (2016).
16. R.E. Banai, H.Lee, S. Zlotnikov, J.R.S. Brownson, and M.W. Horn, *IEEE Photovoltaic Specialists Conference* (2013).
17. M. Devika, N. Reddy, F. Patolsky, and K. Gunasekhar, *J. Appl. Phys.* 104, 12 (2008).
18. R. Banai (Ph.D. dissertation, The Pennsylvania State University, University Park, PA, 2015).
19. O.E. Ogah, K.R. Reddy, G. Zoppi, I. Forbes, and R.W. Miles, *Thin Solid Films* 519, 21 (2011).
20. K.G. Deepa and J. Nagaraju, *Mater. Sci. Semicond. Process.* 27, 649 (2014).
21. R.E. Banai, H. Lee, N.J. Tanen, R.E. Urena, J.J. Cordell, M.W. Horn, and J.R.S. Brownson, *IEEE Photovoltaic Specialists Conference* (2014).
22. M. Gunasekaran and M. Ichimura, *Sol. Energy Mater. Sol. Cells.* 91, 9 (2007).