



Sputter-deposited low loss Mg₂SiO₄ thin films for multilayer hybrids

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ARTICLE INFO

Article history:

Received 17 May 2012

Received in revised form 30 November 2012

Accepted 30 November 2012

Available online 21 December 2012

Keywords:

Magnesium silicate

Magnetron sputtering

Dielectrics

Crystallization

Thin films

X-ray diffraction

Atomic force microscopy

ABSTRACT

Mg₂SiO₄ (forsterite) thin films grown by rf magnetron sputtering from a ceramic target have been investigated particularly for thin film hybrids requiring a low loss dielectric layer. Understanding of the processing parameters and their correlations to dielectric properties is the main concern of this work. Fundamental parameters, such as working pressure and post-deposition annealing temperature, were found to influence phase evolution, morphology and dielectric properties. For example, polycrystalline α-Mg₂SiO₄ could be obtained above the annealing temperature of 500 °C regardless of working pressure. The dielectric constant increased gradually while the dielectric loss showed a reverse trend of decrease with raising annealing temperature to 700 °C. Dielectric constant of ~6.8 and dielectric loss of ~2.8 × 10⁻³ were obtained at 1 MHz from the sample annealed at 700 °C. A promising planarized thin film structure for fine line multilevel packaging was demonstrated without any significant inter-diffusion and damages between Mg₂SiO₄ and Pt layers.

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1. Introduction

Driven by the recent progress in microelectronics packaging, nonconventional dielectric thin film materials have been in demand particularly for high frequency applications such as high speed LAN, intelligent transport system, point-to-point telecommunications, etc. [1,2]. The dielectric thin films need to meet high frequency selectivity and stability, low power dissipation, and the reduced delay time of electronic signal transmission by choosing superior dielectric materials that exhibit an exceptionally low dielectric loss (tanδ) with a reasonably low dielectric constant (*k*) over the broad frequency range [3,4]. However, there have been few studies on dielectric thin films applicable for the high frequency operation at > GHz [5,6]. Among the few candidates for the challenging applications, α-Mg₂SiO₄ (forsterite) may be a great candidate from its competitive dielectric constant of <7.0 and very high *Q*-*f* (quality factor × frequency) value as high as 270,000 GHz as reported in the sintered bulk ceramics [3,7,8]. Only the study dealing with the basic dielectric properties and surface scaling behavior of phase-pure α-Mg₂SiO₄ thin films was recently published by our group [9]. According to the study, loss tangent was shown to decrease up to 1.0 × 10⁻² at 1 MHz with increasing deposition time to 150 min at a fixed deposition temperature of 700 °C, while dielectric constant remained unchanged at the bulk value. As another related study, Kang et al. [10] reported that the thin film of high-pressure polymorphic γ-Mg₂SiO₄ structure was sputter-deposited as a potential buffer layer

on a Si substrate, which was driven by a small lattice mismatch of ~5.48% with the substrate.

In this work, phase-pure α-Mg₂SiO₄ thin films sputter-deposited at room temperature are further investigated for the purpose of understanding the effects of fundamental parameters such as working pressure and annealing temperature on phase evolution, grain growth and dielectric properties. An example of multilayer thin film hybrids consisting of the α-Mg₂SiO₄ thin films and Pt inter-layers is introduced to demonstrate a potential utilization for the upcoming microelectronic packages.

2. Experimental procedure

Thin films were grown on a Pt(111)/Ti/SiO₂/Si(100) substrate at room temperature by rf magnetron sputtering of a 2 inch phase-pure α-Mg₂SiO₄ ceramic target (99.99% purity, LTS Chemical Inc.). In our given sputtering configuration, the substrate was tilted by an angle of ~45° with respect to the target normal. The substrate was ultrasonic-cleaned sequentially with acetone, isopropyl alcohol, and anhydrous ethyl alcohol each for ~10 min prior to the deposition. The sputtering chamber was evacuated to a base pressure of ~6.66 × 10⁻⁴ Pa by a turbomolecular pump. Deposition was conducted at room temperature with a selected working pressure of 1.33, 2.66 or 3.99 Pa (10, 20 or 30 mTorr, respectively) in the fixed condition of 200 W rf power, 120 min deposition time, 6 cm substrate-target separation and 7 RPM substrate rotation rate. The working pressure was controlled by using an Ar/O₂ (3/1) gas mixture through a mass-flow controller. The deposited films were annealed at different temperatures from 300 to 700 °C for 5 min by using an RTA (rapid-thermal

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annealing) system. A multilayer hybrid structure was constructed by depositing the Mg_2SiO_4 film alternately with sputtered Pt inter-electrode and by repeating up to 5 layers of the dielectric film.

Crystalline structure of the films was identified on the basis of X-ray diffraction (XRD) patterns obtained by a PANalytical X'Pert PRO XRD unit using $\text{Cu-K}\alpha$ radiation at the wavelength of 0.154 nm in Bragg–Brentano (θ - 2θ) geometry. Atomic force microscopy (AFM: Nanoscope IIIa system, Digital Instruments) was employed in a semi-contact mode by using an Al-coated Si cantilever to examine surface morphology of the films. Scanning electron microscopy (SEM: S-4700, Hitachi Co., Japan) was operated at 15 kV to determine the thickness of each film and observe cross-sectional image of the multilayer structure. Dielectric properties of the films were measured at room temperature over the frequency range of $\sim 10^3$ to 10^6 Hz at an oscillating voltage of 500 mV by an impedance analyzer (4294A, Agilent) using a metal–insulator–metal structure where a Pt top electrode having a diameter of 250 μm was deposited by DC sputtering.

3. Results and discussion

Fig. 1 shows the variation in the deposition rate of films with increase in working pressure from 1.33 to 3.99 Pa, which was calculated from the obtained thickness value for the fixed deposition time of 120 min. The average thickness of the films was ~ 550 , 405, 360 nm at 1.33, 2.66 and 3.99 Pa, respectively. The deposition rate decreased significantly with increasing working pressure to 3.99 Pa because of the increased collisions of the depositing species with the ambient molecules during their transit inside the deposition chamber as generally recognized. It is noticeable to observe a relatively low deposition rate of ~ 4.6 nm/min even at 1.33 Pa, as compared to the common deposition rate of 10–20 nm/min for oxide compounds [11].

Fig. 2 represents the effect of different working pressures on phase development when the room temperature-deposited film was annealed at 700 °C. All films exhibit only polycrystalline α - Mg_2SiO_4 phase regardless of working pressure although the degree of the α - Mg_2SiO_4 phase tends to decrease slightly with increasing working pressure. Any evidence of phase transition or other secondary phase was not found. There is no report concerning the film formation of the α - Mg_2SiO_4 phase. As the sole study regarding the Mg_2SiO_4 thin films, Kang et al. [10] reported that only (400)-oriented γ - Mg_2SiO_4 structure was found in the higher working pressure range of 6–13 Pa when a Mg target was used for the formation of Mg_2SiO_4 on a Si substrate. In fact, the γ - Mg_2SiO_4 phase in the bulk form is known to exist only at high pressures and elevated temperatures [12,13].

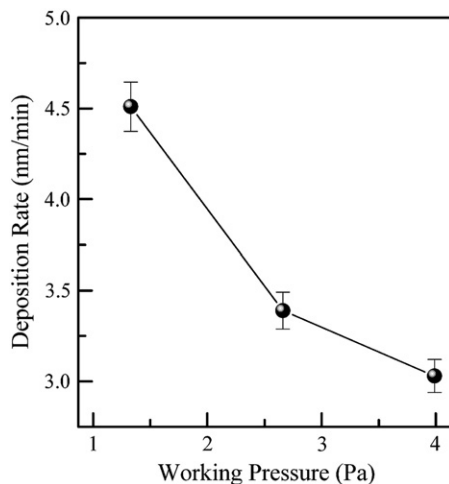


Fig. 1. Plot of deposition rate versus working pressure for the as-deposited Mg_2SiO_4 thin films.

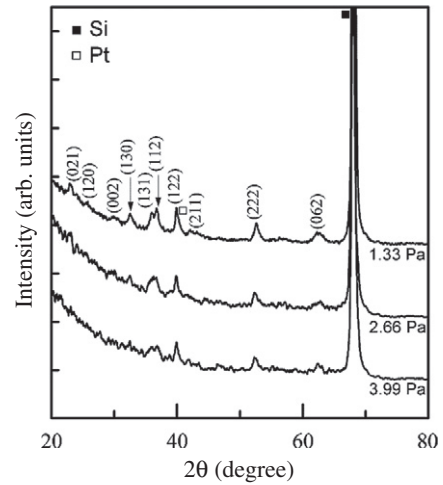


Fig. 2. XRD patterns of Mg_2SiO_4 thin films deposited under different working pressures and annealed at 700 °C.

Fig. 3 shows the effect of different annealing temperatures of 300, 500 and 700 °C on the XRD patterns of Mg_2SiO_4 thin films deposited at 1.33 Pa. All films deposited at room temperature were amorphous regardless of changes in rf power, working pressure and gas flow rate within the proper working range of each parameter. The film remained unchanged as amorphous up to 300 °C. α - Mg_2SiO_4 phase started to crystallize at 500 °C with polycrystalline nature and to evolve further at 700 °C with more distinct appearance of random peaks. Compared to the reported synthesis temperature of ~ 1200 °C for α - Mg_2SiO_4 powders [14], sputtering seems to induce a much lower crystallization temperature, possibly between 300 and 500 °C. Note that the γ - Mg_2SiO_4 phase was not observed even at 700 °C.

The effect of annealing temperature on the surface morphology of the films deposited at 1.33 Pa is shown in Fig. 4. Line profiles of the corresponding AFM images are given in Fig. 4(e). Root mean square (RMS) roughness and grain height, which were quantitatively observed from the AFM images, are presented in Fig. 5. The grain height of the film tended to increase with increase in the annealing temperature because of the stronger development of crystallization during annealing. This tendency was also correlated well to the variation in surface roughness of the films as the increase of RMS roughness from ~ 2.7 to 6.6 nm was observed with increasing annealing temperature. The roughness increase is likely limited to the dominance of lateral growth of grains of α - Mg_2SiO_4 and, presumably, to the extended

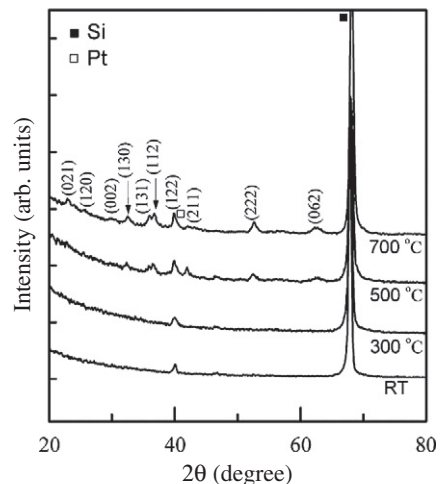


Fig. 3. XRD patterns of Mg_2SiO_4 thin films deposited at 1.33 Pa at room temperature and annealed at different temperatures.

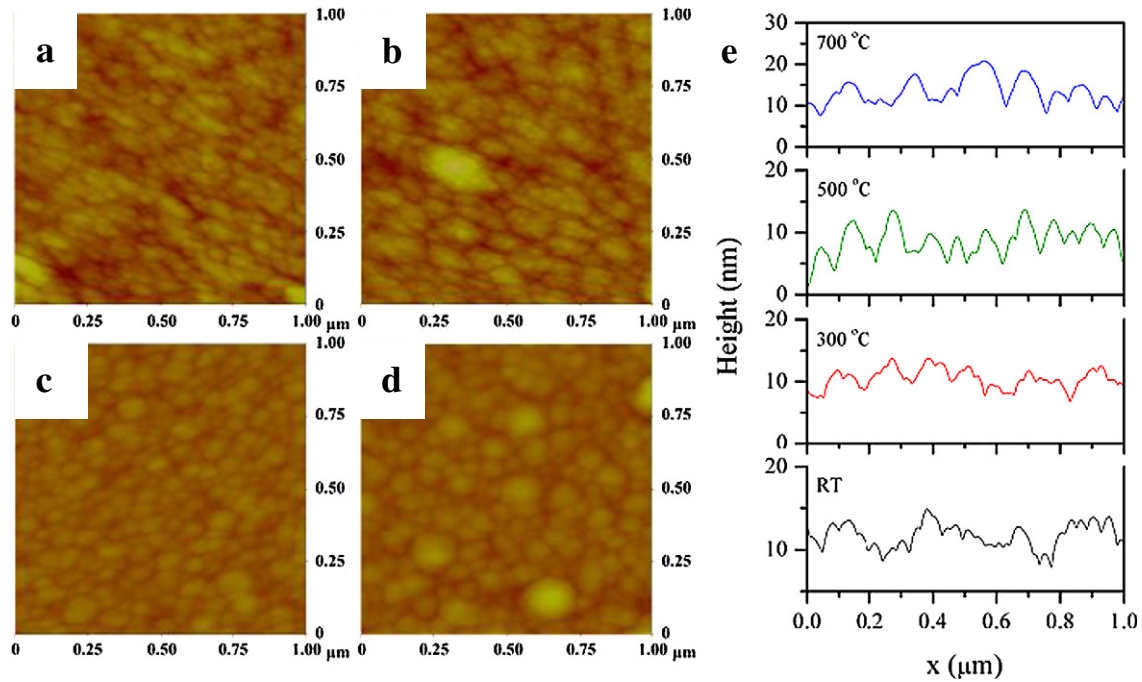


Fig. 4. AFM surface images (1 μm × 1 μm) of (a) as-deposited film and the films annealed at (b) 300, (c) 500 and (d) 700 °C. Surface profiles at different annealing temperatures are shown in (e).

densification of thin films while minimizing surface energy at the elevated temperature.

The variation of grain size with annealing temperature is depicted in Fig. 6. The grain size turned out to increase significantly after 300 °C and reached at ~82 nm at 700 °C. This behavior may be acceptable in that a higher temperature usually provides a higher driving force for grain growth as long as the grain growth is not limited by the film thickness [15]. Since this high temperature of 700 °C corresponds to the region of active growth towards random orientation, the evolvement of continuing structural ordering with a sufficient driving force may simultaneously affect the secondary crystallization (or recrystallization) of growing grains.

Fig. 7 shows the dielectric constant and dielectric loss measured at 1 MHz as a function of annealing temperature for the films deposited at 1.33 Pa. The thickness of the annealed films was changed from ~550 nm of the as-deposited film into 543, 539 and 532 nm at 300, 500 and 700 °C, respectively. The dielectric constant increased

gradually from ~4.1 for the as-deposited film to ~6.8 at 1 MHz with raising the temperature to 700 °C. As commonly accepted, the observed low dielectric constant in the amorphous state is believed to be due to numerous defects from incomplete structural ordering and limited surface diffusion of the sputtered species [16]. As the film proceeds with intense crystallization of the α-Mg₂SiO₄ phase, dielectric constant seems to approach to the expected value of ~6.8 similar to that of the bulk counterpart [8]. The dependency of crystal directionality of the dielectric constant is not expected due to the random orientation (or polycrystalline nature) of these films at high temperatures. Although it is not clear about the degree of sensitivity of *k* to grain size, strong crystallinity of α-Mg₂SiO₄ achieved at the high temperature of 700 °C is likely to be a more probable reason for this increased *k* value. There is a report in dealing with grain boundary influence of this bulk material on dielectric properties, which suggests that the grain boundary even with segregation of impurities does not affect dielectric constant seriously [17].

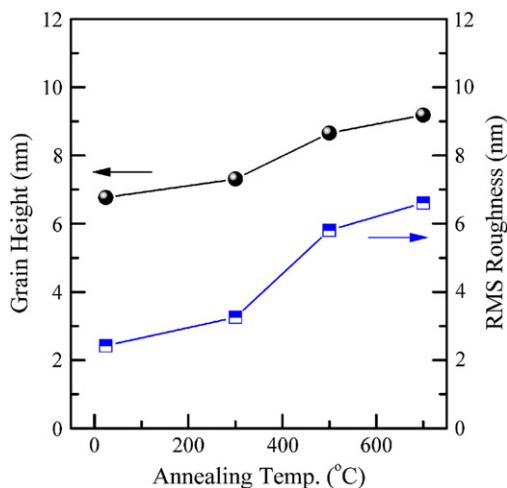


Fig. 5. Grain height and root mean square roughness as a function of annealing temperature for the Mg₂SiO₄ thin films. The films were grown at 1.33 Pa.

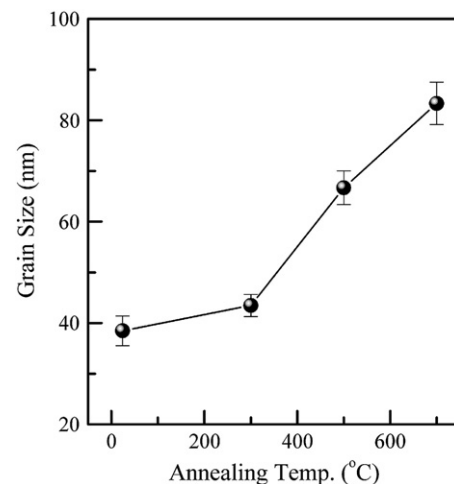


Fig. 6. Variation in grain size with increasing annealing temperature for the Mg₂SiO₄ thin films. The films were grown at 1.33 Pa.

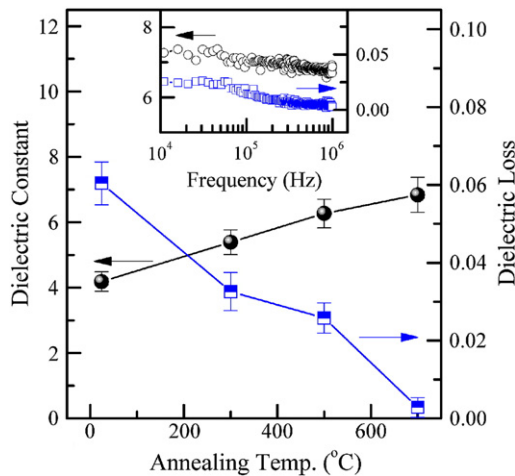


Fig. 7. Dielectric constant and loss tangent ($\tan\delta$) as a function of annealing temperature for the Mg_2SiO_4 thin films deposited at 1.33 Pa. Variations of the dielectric properties with frequency are shown as inset.

The relationship between the dielectric loss and annealing temperature is quite opposite with the trend in dielectric constant. The amorphous state of the thin films annealed at room temperature shows a higher loss value. The transformation from amorphous to crystalline phase caused dielectric loss to decrease gradually. The strong crystallinity of $\alpha\text{-Mg}_2\text{SiO}_4$ at 700 °C seems to eventually help reducing the dielectric loss up to the level of $\sim 2.8 \times 10^{-3}$ at 1 MHz due to the better structural ordering with less defects. This minimum value at the annealing temperature of 700 °C is much lower than $\sim 1.0 \times 10^{-2}$ for $\alpha\text{-Mg}_2\text{SiO}_4$ films deposited at the substrate temperature of 700 °C as reported previously [9]. It suggests that the annealing process is more effective in producing lower loss tangent than the deposition at the identical substrate temperature. Even compared to the reported loss tangent values (usually $> 1\text{--}10\%$) for other oxide thin films, this loss tangent value of $\alpha\text{-Mg}_2\text{SiO}_4$ films is quite competitive [18].

The frequency dependency of the dielectric constant and loss of the films annealed at 700 °C is shown as inset in Fig. 7. The dielectric constant and dielectric loss showed no noticeable dispersion characteristics on frequencies up to ~ 1 MHz, indicating no dielectric relaxation or no actual frequency dependence of the films at least over the $\sim 10^3$ to 10^6 Hz range. The least frequency-dependent dielectric properties might be expected from the paraelectric nature of the material, where no dramatic variation of k is a usual feature at least over the corresponding frequency range up to $\sim 10^6$ Hz [19]. Although the similar low level of loss tangent at GHz frequency is hardly assumed without the actual measurement, $\alpha\text{-Mg}_2\text{SiO}_4$ film is still regarded as a good candidate for high frequency applications as long as a high quality film can be fabricated without detrimental structural defects and/or signal interference from contacting layers.

A potential hybrid structure of $\text{Mg}_2\text{SiO}_4/\text{Pt}$ multilayer films deposited at room temperature on a Pt(111)/Ti/SiO₂/Si(100) substrate by a continuous process without breaking vacuum is demonstrated in the SEM image of Fig. 8. The multilayer structure defines well each layer of the dielectric thin film with inter-layered metallization. There is neither inter-diffusion nor noticeable crack at interfaces as confirmed even after annealing at the high temperature of 700 °C. It suggests that this type of structure may be an ideal solution for coming thin film-based hybrid packages since this dielectric thin film provides exceptionally low dielectric loss of $< 1\%$ even in the amorphous state. It should be mentioned that the dielectric properties obtained in Fig. 8 may not be directly applicable for the multilayer structure due mainly to the internal signal interference, extra interfaces, and higher density of potential defects/damages although the intrinsic

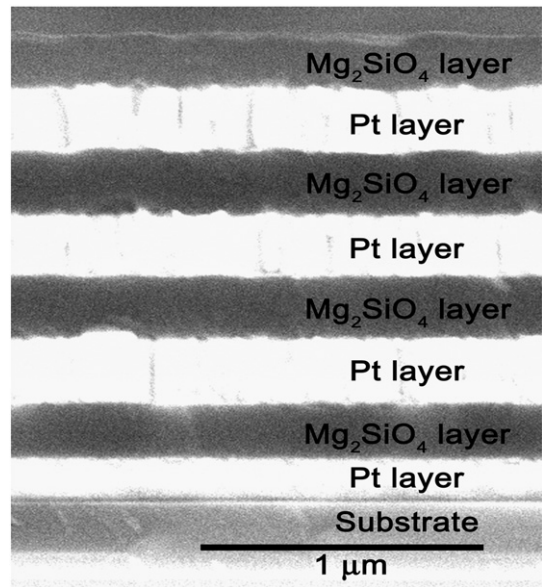


Fig. 8. Cross-sectional SEM image of an example of multilayered Mg_2SiO_4 -based thin film hybrid structure with Pt inter-layers.

low loss characteristics of $\alpha\text{-Mg}_2\text{SiO}_4$ are expected to affect positively the performance of such multilayer hybrids.

4. Conclusions

Sputter-deposition of $\alpha\text{-Mg}_2\text{SiO}_4$ thin films was investigated for the potential utilization of hybrid packages requiring extremely low dielectric loss of $< 10^{-2}$. The appearance of phase-pure polycrystalline $\alpha\text{-Mg}_2\text{SiO}_4$ seemed to be limited by certain deposition conditions, i.e., the low working pressure of ~ 1.33 Pa and the high annealing temperature of ~ 700 °C. The strong dependence of the degree of crystallization, surface morphology and dielectric properties on annealing temperature was observed as a key achievement of this work. A promising planarized multilayered structure for potential thin film hybrids was demonstrated as an ultimate example of incorporating the low loss dielectric thin film.

Acknowledgments

This work was supported by a grant from the Ministry of Knowledge Economy, Korea, specified by the Foundation R&D Program for Core Technology of Materials, and also partially by the National Research Foundation of Korea (NRF) grant funded by the Ministry of Education, Science and Technology (No. 2011-0017983 and 2011-0020285).

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